PRODUCT SUMMARY
R & D ELECTRONICS (PTY) LTD

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QBX-PCC
PARALLEL I/O, CLOCK AND JULIAN CALENDAR

clock and Julian calendar
up to 13 buffered I/O lines
on board battery backup
full speed iSBX bus compatible
periodic interrupt capability

The QBX-PCC is an iSBX compatible module providing time and date information for a host computer. The information provided is seconds, minutes, hours, date, day of week, and month. Through software it is possible to include leap year adjustments and a facility for years. An on-board 40 bit shift register may store information in power fail situations.

In addition to the clock function up to 13 buffered I/O lines are provided. They consist of Port A and 5 bits of Port C of the Intel 8255A-5 peripheral device.
The remainder of this device is used to interface to the clock. It also allows interface to the SBX bus without wait state generation.

QBX-FOG/C
HARDWARE STACK AND NON VOLATILE RAM

non-volatile storage on iSBX* bus
organised as a hardware stack
256 bytes
any address may be accessed
stack counter value can be read
provision for off board standby battery
on board wait state generator

The QBX-FOG/C provides an ideal method of non-volatile storage for iSBC computers. The 256 bytes are configured as a hardware stack which allows added software flexibilty to a system in terms of parameter passing in subroutines. It also saves memory space since it occupies 16 I/O locations if configured as I/O mapped I/O.

The RAM may be accessed by programming an address on the stack counter and then "pushing" to write and "popping" to read. Each "push" or "pop" automatically updates the stack counter. Since the write or read functions occupy only one I/O location DMA techniques may be used to transfer blocs of data. An on board wait state generator allows full speed operation of the micro-processor.

The non-volatility of course means that various parameters may be stored during a power fail.

QBX-FOG/E
HARDWARE STACK AND NON-VOLATILE EEPROM

non-volatile storage on iSBX bus
organised as a hardware stack
64 (QBX-FOG/E-64) or 256 (QBX-FOG/E-256) bytes of RAM and "shadow" EEPROM
any address may be accessed
stack operation immeditely updates memory address
5V only EEPROM
on board wait state generator

The QBX-FOG/E provides an ideal method of non-volatile storage for iSBC computers. The memory is configured as a stack, but random access is possible to any stack location. The memory has two portions, RAM with a "shadow" EEPROM. There is a bit for bit correalation from the RAM to the EEPROM. Saving the RAM in the EEPROM overwrites the contents of the EEPROM with an identical image of the RAM. Recalling the EEPROM overwrites the contents of the RAM with an identical image of the contents of the EEPROM. The RAM may be used for normal storage operations as well. See the QBX-FOG/E users manual for possible applications.

The RAM may be accessed by programming an address on the stack counter and then "pushing" to write and "popping" to read. Each "push" or "pop" automatically updates the stack counter. When mounted in a connector configured as I/O mapped I/O the module occupies no memory space. An additional stack can also provide many advantages. Since the write or read functions occupy only one I/O location DMA techniques may be used to load or unload blocs of data. An on board wait state generator allows full speed operation of the microprocessor.

QBX-MSP
MULTI SERIAL PORT

2 (QBX-MSP/2) or 4 (QBX-MSP/4) asynchronous channels
uses Western Digital WD2123 devices
16 independent baud rates for each channel (50-19200 baud)
5-8 bits per character
1, 16, or 64 times clock rate sampling
line break detection and generation
odd and even parity generation and detection
double buffering of data
overrun and framing error detection
asynchronously compatible with industry standard 8251A
diagnostic local loop back mode
iSBX bus compatible (double sized board)
interrupt generation

on board wait state generation
RS232 voltage level drivers and receivers
QBN-MSP-CON available to provide connection to normal D-type connector

The QBX-MSP allows 2 or 4 asynchronous ports on a double sized SBX module. Each port has an individually programmed baud rate generator that allows transmission rates from 50 to 19200 baud. Once set up, the handling of the control and data ports is compatible with most software written for the 8251A serial communications controller in the asynchronous mode. A facilty exists for a local loop back test and interrupt gating is provided to generate an interrupt to the host processor. An on board wait state generator allows full speed operation of the microprocessor.

QBX-TMR
MULTI FUNCTION TIMING CONTROLLER

Sophisticated Timing Controller on single SBX* card.
5 independent 16 bit counters
High speed counting rates
Up/down and Binary/ BCD counting
Internal/external frequency source with tapped frequency scaler
Programmable frequency output
Time of day option
Alarm comparators on counters 1 and 2
Counters may be internally concatenated
Complex duty cycle outputs
One shot or continuous outputs
Programmable counter source selection
Programmable input and output polarities
Programmable gating
Retriggerable
Inputs overvoltage protected
Outputs buffered by Darlington transistors

Counting events and timing intervals are fudamental to many microcomputer projects. If the computer is required to execute several of these functions simultaneously in software, the time available for other requirements can become severely limted. By allowing these functions to be executed in hardware improves the situation considerably.

The QBX-TMR provides the Multibus user with these facilities by placing one of the most sophisticated timing controllers, the Am9513 on a single sized SBX card. This device has 5 independent 16 bit counters which may even be internally concatenated in stages to allow up to an 80 bit counter. For each counter there are 16 possible counter inputs selected by software. They include any of 5 source inputs, any of 5 gate inputs, or a selection from a the divided outputs of an external oscillator.

Up to 10 gates exist to allow modification of the counting patterns to generate monostable, FSK generation and many other functions. The input and output polarities are programmable.

The inputs are protected by a zener diode and series resistor whilst the outputs are buffered by Darlington drivers allowing medium voltage and current interface.
Interrupts are also catered for, and a latch exists to store transient pulses.

QBC-QBX
Quad SBX Module MULTIBUS Board

Uncommitted MULTIBUS board
Supports up to 4 SBX 8 bit modules
Memory Mapped or I/O mapped I/O
Address space to 20 bits
Programmable XACK response time
Configured as 8 bit MULTIBUS slave
IEEE P796 Bus Compliance: D8 M20 I16 VO L
Unoccupied modules do not occupy memory or I/O space
Does for the SBC card what the (E)PROM did for the ROM

The SBX bus introduced by Intel has allowed considerable flexibility in configuring MULTIBUS systems. Each module represents a specifc function and is used only when needed. This reduces the "overkill" of having to add a full size MULTIBUS card with unwanted functions. Only the newer MULTIBUS CPU cards have three connectors whilst others have less or even none. This means that if a function is required beyond the SBX capabilty of the host CPU board, a new card is needed, and so the advantage of the SBX modules is lost. The QBC-QBX addresses this problem.

The QBC-QBX is merely a host board for up to 4 SBX compatible boards (4 single, 3 single and 1 double, or 2 single and 2 double). It allows the board to be configured as a MULTIBUS slave, memory mapped or I/O mapped I/O. It will only support 8 bit SBX modules, but as 16 bit bus masters can handle 8 bit transfers this is not seen as a problem. As memory mapped I/O up to 20 bits of address may be decoded.

The QBC-QBX allows shared SBX facilities in a multiprocessor environment on the MULTIBUS. It also allows the retrofit of SBX modules to existing projects and even the use of stock (or cheaper) CPU boards that do not support the SBX bus on new projects.

QBX-FST
FAILSAFE TIMER

Dual monostable Failsafe Timer
Each monostable has separate address
Cold start / warm start detection
Visual indication of failsafe reset
Enable for external devices e.g. solenoids
AC low detection
Uncommitted single bit output
Outputs buffered by Darlington transistors

Almost any application involving microcomputers should include a failsafe timer for totally reliable operation. The cost associated with correcting erratic computer behaviour, be it due to unusual combination of input variables or simply radiated electronic noise, is normally very high. It requires a large number of man hours to wait for the fault that occurs only sporadically and unpredictably and ties up equipment that could be used more profitably elsewhere.

The principle of a failsafe timer is that periodically the microcomputer must signal the timer that it is functioning properly and delay consequential action for a further set period. If a failure occurs a reset pulse is generated and the processor is restarted. In this set of circumstances it may be necessary for the microcomputer to "know" whether it has just been switched on or if, in fact, a failure did occur. Expierience has also shown that even in a failed condition a system can still clock a failsafe timer.

The QBX-FST addresses all these problems within the Multibus environment. It provides two failsafe timers that are combined to generate a reset signal whenever either "times out". As a further level of security these two monstable timers are at different I/O locations and both require a 2 stage operation to restart the timer. In addition the QBX-FST also has the capabilty of providing information on whether the reset was due to switching on (cold start) or due to a failure reset (warm start). This information is also presented on Light Emitting Diodes for the system designer and the commissioning engineer can interpret the effects being observed.

On many systems where external devices such as solenoids and relays are controlled by the host computer these devices may behave in an unwanted manner until conditions in the computer (at switch on) have stabilised. On computer failure other unwanted conditions may arise. The QBX-FST has an output derived from the failsafe timers that will enable these devices only when they should be, and will turn them off on failure.

With the available board space a detector for AC low is implemented on the QBX-FST as well as a single bit buffered output for user convenience.